

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

Applicant: PARK, JIN-HO )  
Serial No. 10/756,939 ) Group Art Unit: 2629  
Filed: January 14, 2004 )  
For: LIQUID CRYSTAL DISPLAY APPARATUS ) Examiner:  
 ) WILLIAM BODDIE  
 ) Confirmation No.: 3289  
 )

**PRE-APPEAL BRIEF REQUEST FOR REVIEW**

In response to the Office action mailed November 3, 2009, in conjunction with the Notice of Appeal filed concurrently herewith, Applicant submits the following remarks in support of the Pre-Appeal Brief Request for Review:

**REMARKS**

The present submission is responsive to the Office action of November 3, 2009 (hereinafter referred to as “instant Office Action”), in which Claims 1-11 and 14-17 are presently pending.

In the instant Office action, Claims 1-5, 7-9 and 14-17 are rejected under 35 U.S.C. § 103(a) as being allegedly unpatentable over Kawaguchi et al., U.S. Patent No. 5,592,199 (hereinafter “Kawaguchi”) in view of Nakamura et al., U.S. Patent No. 7,136,058 (hereinafter “Nakamura”). Claims 6 and 10 are rejected as being allegedly unpatentable over Kawaguchi in view of Nakamura, and further in view of Kubota et al., U.S. Patent No. 6,791,526. Applicant respectfully traverses the §103 claim rejections for the reasons stated below.

Independent **Claims 1 and 7** similarly recite, *inter alia*:

“an output instruction signal line disposed on the second substrate and opposing the common electrode;

a timing controller providing a first control signal to the gate driver so as to control an output of the gate driving signal, and providing an output instruction signal to the data driver via the output instruction signal line to delay the output instruction signal depending on a capacitive load and a resistive load formed by the output instruction signal line and the common electrode,

wherein the data driver outputs a delayed image data signal to the LCD panel as the output instruction signal is delayed such that a delayed time of the image signal is substantially equal to a delayed time of the gate driving signal.”

In the instant Office action at Page 2, it is stated that “Kawaguchi is seen to provide a resistive load on the output instruction signal line [common line, 231, Figures 30-32], which in turn imparts an *inherent yet undefined* amount of delay. Furthermore, the delay of the gate lines, which is substantially caused by both resistive and capacitive loads, is not equivalent to the amount of delay of the output instruction signal line

of Kawaguchi. In other words, Kawaguchi's disclosure results in an *inherent output instruction signal delay* due solely to the resistive properties of the signal line itself. However, this delay, caused by the resistive properties alone, is *not equivalent to the delay of the gate signal.*" It is then concluded in the instant Office action that the "delay of the gate signal of Kawaguchi is caused by not only a similar resistive load as the output instruction signal, but also a capacitive load which is caused by *the arrangement of the common electrode and the gate line.*" However, regarding Kawaguchi, it is then conceded at Pages 5 and 9 of the instant Office action that "*a common electrode disposed on the first substrate*" or the common line 231 (as the "output instruction signal line") opposing a *common electrode*, as claimed, is not taught or suggested by Kawaguchi.

To provide a "common electrode," Nakamura is relied upon as allegedly teaching a common electrode disposed on the first substrate and opposing signal line. In the instant Office action at Page 3, it is stated that "[w]hile Examiner agrees that Nakamura *does not expressly disclose a timing effect*, there will *nonetheless be a delay* caused by both the resistive and capacitive loads formed by the metallic material of the signal line electrode and the arrangement of the electrodes, respectively."

It is then concluded on Pages 3, 6 and 10 of the instant Office action, that upon combining the common line 231 of Kawaguchi allegedly teaching an *inherent yet undefined* amount of delay, under the common electrode taught by Nakamura which *does not teach any timing effect*, a structurally similar display to the claimed invention results and the delay time of the image signal will be *substantially equal* to a delayed time of the gate driving signal. That is, the instant Office action concludes without any further explanation that an "undefined amount" of delay of Kawaguchi, and specifically a delay of the gate lines which *is not equivalent to the amount of delay of the output instruction signal line*, added or combined with *no timing effect* of Nakamura specifically equals the "*substantially equal*" delay of signal lines of the claimed invention. Applicant respectfully disagrees.

Firstly, while conceding that neither Kawaguchi and Nakamura teaches or suggests a defined "timing delay" or "timing effect," it is nonetheless asserted for both Kawaguchi and Nakamura, that there is an "inherent" timing delay, and more specifically, a timing delay where "the data driver outputs a delayed image data signal to the LCD panel as the output instruction signal is delayed *such that a delayed time of the image signal is substantially equal to a delayed time of the gate driving signal,*" as claimed. Applicant respectfully disagrees.

The theory of inherency is normally reserved for rejections under 35 U.S.C. § 102. *In re Grasseli*, 318 U.S.P.Q. 303 (Fed. Cir. 1983). In order to support an anticipation rejection based on inherency, an Examiner must provide factual and technical grounds establishing that the **inherent feature necessarily**

**flows from the teachings of the prior art.** (Emphasis added) *Ex parte Levy*, 17 U.S.P.Q.2d 1461, 1464 (Bd. Pat. App. & Int. 1990).

Applicant respectfully submits that no factual or technical grounds have been provided in the rejection details, establishing that the “*delayed time of the image signal is substantially equal to a delayed time of the gate driving signal*” of the claimed invention *necessarily flows* from the teachings in Kawaguchi of an “undefined amount” of delay and specifically a delay of the gate lines which *is not equivalent to the amount of delay of the output instruction signal line*, and from the teaching in Nakamura of *no timing effect*. To the contrary, it is merely concluded based on inherency, that an “undefined amount” of delay of Kawaguchi, and specifically a delay of the gate lines which *is not equivalent to the amount of delay of the output instruction signal line*, added or combined with *no timing effect* of Nakamura specifically equals a “*substantially equal*” delay of signal lines. Accordingly, the rejection under §103 based on inherency is improper and should be withdrawn.

Furthermore, it is respectfully submitted that the Examiner has used Applicant’s disclosure to select portions of the cited references to allegedly arrive at Applicant’s invention. In doing so, the Examiner has failed to consider the teachings of the references or Applicant’s invention as a whole in contravention of section 103, including the disclosures of the references which teach away from Applicant’s invention.

Where Kawaguchi specifically teaches a delay of the gate lines which *is not equivalent to the amount of delay of the output instruction signal line*, contrary to the claimed invention, and Nakamura teaches *no timing effect* of Nakamura, such teachings provide no suggestion or motivation for a “*delayed time of the image signal is substantially equal to a delayed time of the gate driving signal*” of the claimed invention. Therefore, Applicant respectfully submits that the teaching of the references have not been considered in contravention of section 103, that Applicant’s disclosure has been used as an instruction manual or ‘template’ to piece together the teachings of the prior art so that the claimed invention is allegedly rendered obvious, and that the rejection under §103 is further improper and should be withdrawn.

Secondly, for all the reasons discussed on Page 7, line 1 to page 8, line 14 of the previously filed response of September 3, 2009 to Non-Final Office action of June 3, 2009, Applicant respectfully submits that since Kawaguchi does not disclose, teach or suggest an *intentional delay*, and since any such delay of a signal line can only be asserted on grounds of “*inherency of an undefined delay*” due to the material of the signal line, more specifically a delay of the gate lines which *is not equivalent to the amount of delay of the output instruction signal line*, there exists *no teaching, suggestion or motivation* with respect to Kawaguchi regarding providing an output instruction signal to the data driver via the output instruction signal line to delay the output instruction signal depending on a capacitive load and a resistive load formed by the

output instruction signal line and the common electrode, and the data driver outputs a delayed image data signal to the LCD panel as the output instruction signal is delayed such that a delayed time of the image signal is substantially equal to a delayed time of the gate driving signal of independent Claims 1 and 7.

Thirdly, referring to the discussion on Page 8, line 16 to page 9, line 14 of the previously filed response of September 3, 2009 to Non-Final Office action of June 3, 2009, since *no timing affect* is taught or suggested by the structure of Nakamura including the common electrode, when such a structure is combined with the structure of Kawaguchi teaching *an undefined delay*, and specifically a delay of the gate lines which *is not equivalent to the amount of delay of the output instruction signal line*, the combined structure and the references provide *no teaching, suggestion or motivation* of at least a delayed time of the image signal is substantially equal to a delayed time of the gate driving signal, as claimed.

Particularly, P1 illustrated in FIG. 14 of Nakamura is a *power supply line* of an AMP, and an overlapped portion illustrated in FIG. 15 is a *capacitor* of an AMP. Thus, even if signals of *the power supply line P1 and the capacitor* are delayed, a delayed time of an image data signal *cannot be substantially equal to a delayed time of a gate driving signal*. Thus, the power supply line P1 and the capacitor of Nakamura are different from the “output instruction signal line,” as claimed. Therefore, there further exists *no teaching, suggestion or motivation* to modify or combine at least Kawaguchi and Nakamura to teach a delayed time of the image signal is substantially equal to a delayed time of the gate driving signal, as claimed.

Fourthly, it is asserted on Pages 6 and 10 of the instant Office action that the motivation for arranging the signal lines of Kawaguchi so as to overlap the common electrode as taught by Nakamura would be to reduce the frame size of the LCD, resulting in a more portable display, as evidenced by Col. 15, lines 42-50 of Nakamura. Applicant respectfully disagrees.

For all the reasons discussed on Page 9, line 15 to page 10, line 9 of the previously filed response of September 3, 2009 to Non-Final Office action of June 3, 2009, Applicant respectfully submits that there exists *no suggestion or motivation* in the references or to one of ordinary skill in the art to modify or combine Kawaguchi and Nakamura to provide an output instruction signal to the data driver via the output instruction signal line to delay the output instruction signal depending on a capacitive load and a resistive load formed by the output instruction signal line and the common electrode, and the data driver outputs a delayed image data signal to the LCD panel as the output instruction signal is delayed such that a delayed time of the image signal is substantially equal to a delayed time of the gate driving signal of independent Claims 1 and 7.

Finally, referring to the discussion on Page 10, line 11 to page 11, line 15 of the previously filed

response of September 3, 2009 to Non-Final Office action of June 3, 2009, Applicant respectfully submits that the teachings of Kubota *do not provide the teaching, suggestion or motivation for providing an output instruction signal to the data driver via the output instruction signal line to delay the output instruction signal depending on a capacitive load and a resistive load formed by the output instruction signal line and the common electrode* of amended independent Claims 1 and 7, and do not remedy the deficiencies of Kawaguchi and Nakamura discussed above.

Thus, Applicant respectfully submits that for all the reasons above, Kawaguchi, Nakamura and Kubota, alone or in combination, *fail to teach or suggest all of the limitations* of at least independent Claims 1 and 7, and Claims 2-6, 8-11 and 14-17 as depending upon Claims 1 and 7, and there exists *no suggestion or motivation to modify or combine the references* to teach the claimed invention. Accordingly, *prime facie* obviousness does not exist regarding Claims 1-11 and 14-17 with respect to Kawaguchi, Nakamura and Kubota.

For the above stated reasons, it is respectfully submitted that the rejection of Claims 1-11 and 14-17 is in error and that the same are allowable over the art of record. The fee set forth in 37 CFR 41.20(b)(1) is enclosed herewith. However, if any fees are due with respect to this submission, please charge them to Deposit Account No. **06-1130** maintained by Applicant's attorneys. Applicant hereby petitions for any necessary extension of time required under 37 C.F.R. 1.136(a) or 1.136(b) which may be required for entry and consideration of the present Reply.

Respectfully submitted,

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